UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,494	07/11/2003	Graham Clift	50T5348.01	2833

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EXAMINER
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ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 July 2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-23_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-4,6,9-12 and 16-20_ is/are rejected.

7)☒ Claim(s) _5,7,8,13-15 and 21-23_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _11 July 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _07/11/2003_.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

Claim Objections

1.   Claims 1-2, 5, 17, 21, and 23 are objected to because of the following informalities:

Re claim 1, the applicant is advised to rewrite the phase "wcounter stages" in line

2 as "w counter stages" for clarification. Claim 17 has the same objection.

Re claim 2, the applicant is advised to replace the acronym "an ASIC" in line 2 as

"an application specific integrated circuit (ASIC)" for clarification. Re claims 11 and 18

have the same objection.

Re claim 5, the applicant is advised to rewrite the phrase "(an AND of a previous

count bit and a previous carry bit)" in lines 3-4 as "an output of an AND of a previous

count bit and a previous carry bit" for clarification. Re claims 21 and 23 have the same

objection.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1-2, 4, 6, 16-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated

by Ivo Viscor ("Gray Counter in VHDL").

Re claim 1, Ivo Viscor discloses in Figures 1-2 a data bit counter having a width
"w" (e.g. gray counter in Figure 2 with the width is 3), comprising: at least wcounter
stages (e.g. three gray_1 stage in the Figure 2), each stage (e.g. take the middle gray_1 in
Figure 2) receiving at least one carry bit (e.g. Z(1) as the carry-in into the middle gray_1
in Figure 2), and at least one count bit (e.g. the Qout from the right gray_1 to the middle
gray_1 in Figure 2), each stage (e.g. take the middle gray_1 in Figure 2) executing logic
on the count bit and carry bit to output at least one count bit (e.g. Qout of the middle
gray_1 to the next gray_1 in Figure 2) and at least one carry bit (e.g. Z(2) as Zout as the
carry out bit of the middle gray_1 in Figure 2) to a next highest stage (e.g. the last gray_1
in Figure 2), the count bits output by the stages together representing a Gray counter
count value (e.g. last line in page 1 to the first line in page 2).

Re claim 2, Ivo Viscor further discloses in Figures 1-2 the counter is embodied on
at least one of: a field programmable gate array, and an ASIC (e.g. introduction section in
page 1 first paragraph wherein the Gray counter is implemented in VHDL as part of
ASICs).

Re claim 4, Ivo Viscor further discloses in Figures 1-2 the logic for outputting a
carry bit includes determining an AND (e.g. the bottom AND gate with symbol & in
Figure 1 as gray_1) between an input carry bit (e.g. Zin as the carry-in input from the
previous gray_1) and an inverted input count bit (e.g. qin as count-in is inverted with the
circle prior entering the AND gate in Figure 1).

Re claim 6, Ivo Viscor further discloses in Figures 1-2 the logic includes changing
a Gray code counter bit when both the previous count bit and previous carry bit have

values equal to one (e.g. this is the property of T-flipflop of the gray_l counter in Figure
1 wherein when both the carry-in as Zin and count-in as qin are equal to one, T will be
equal to 1 according to AND gate, then the output of the T flip-flop as qout must be
flipped/changed state).

Re claim 16, Ivo Viscor discloses in Figures 1-2 a logic device executing method
acts for counting a number of bits processed (e.g. Figures 1-2, abstract, and the
paragraphs under the description of the Gray counter in VHDL section in pages 1-2), the
method acts comprising: generating a carry bit chain (e.g. Zout of each gray_l node in
Figure 2) useful for determining which, if any, higher order bits should change in a next
clock cycle (e.g. Zin from the previous gray_l node is AND with Qin from the previous
gray_l node to determine whether or not the Qout should change); generating a count bit
chain (e.g. Qout of each gray_l node in Figure 2), the chains being dependent on each
other (e.g. all gray_1s are depend on each other to determine the gray counting); and
using the count bit chain to indicate a count of a number of bits (e.g. last line of page 1 to
first line of page 2 and the output of q(1) to q(3) in Figure 2 in page 2).

Re claim 17, it has same limitations cited in claim 1. Thus, claim 17 is also
rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 18, it has same limitations cited in claim 2. Thus, claim 18 is also
rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 20, it has same limitations cited in claim 4. Thus, claim 20 is also
rejected under the same rationale as cited in the rejection of rejected claim 4.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 3, 9-12, and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Ivo

Viscor ("Gray Counter in VHDL") in view of Hsu et al. (U.S. 6,845,414).

        Re claim 3, Ivo Viscor fails to disclose in Figures 1-2 the gate array is

implemented in a computer device having at least a main processor and at least a

communication processor communicating therewith. However, Hsu et al. disclose in

Figures 2 and 5-8 the gate array as gray counter (e.g. col. 2 lines 24-30 and Figures 5-6)

is implemented in a computer device having at least a main processor (e.g. lower portion

of Figure 2 and right portion of Figure 5 as read processor) and at least a communication

processor communicating therewith (e.g. upper portion of Figure 2 and left portion of

Figure 2 as write processor). Therefore, it would have been obvious to a person having

ordinary skill in the art at the time the invention is made to add the gate array is

implemented in a computer device having at least a main processor and at least a

communication processor communicating therewith as seen in Hsu et al.'s invention into

Ivo Viscor's invention because it would enable to efficiently control the access between

the processors as read processor and write processor (e.g. abstract, col. 1 lines 12-25, and

col. 2 lines 16-41).

Re claim 9, Ivo Viscor discloses in Figures 1-2 a computing device (e.g.

introduction section in page 1 and first paragraph under the description of the gray

counter in VHDL section in page 1), comprising: at least one Gray code counter (e.g.

second paragraph under the introduction section page 1 and Figures 1-2 wherein the q(1)-

q(3) are the output of the gray counter in Figure 2), the counter being generic in width

(e.g. second paragraph under the description of the gray counter in VHDL section in page

1 and part of code lines 6-11 page 5) and having a reset value that is undetermined at

compilation (e.g. part of code lines 22-33 of page 4 and part of code lines 32-43 of page 5

wherein the reset value is not fixed but rather it is depending on the clock and other

signals as seen in part of code in page 4, thus, the value of reset q(0) is not determined at

the compilation time). Ivo Viscor fails to disclose at least one main processor; at least

one communication processor; and at least one data buffer associated by the gray counter

between the processors for transferring data there between. However, Hsu et al. disclose

in Figures 2 and 5-8 at least one main processor (e.g. lower portion of Figure 2 and right

portion of Figure 5 as read processor); at least one communication processor (e.g. upper

portion of Figure 2 and left portion of Figure 2 as write processor); and at least one data

buffer associated by the gray counter (e.g. part 510 in Figure 5 and col. 3 line 59 to col. 4

line 17) the between the processors for transferring data there between (e.g. Figure 5

wherein the data are transferred across the left and the right part of Figure 5). Therefore,

it would have been obvious to a person having ordinary skill in the art at the time the

invention is made to add at least one main processor; at least one communication

processor; and at least one data buffer associated by the gray counter between the

processors for transferring data there between as seen in Hsu et al.'s invention into Ivo

Viscor's invention because it would enable to efficiently control the access between the

processors as read processor and write processor (e.g. abstract, col. 1 lines 12-25, and col.

2 lines 16-41).

Re claim 10, it has same limitations cited in claim 1. Thus, claim 10 is also

rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it has same limitations cited in claim 2. Thus, claim 11 is also

rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 12, it has same limitations cited in claim 4. Thus, claim 12 is also

rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 19, it has same limitations cited in claim 3. Thus, claim 19 is also

rejected under the same rationale as cited in the rejection of rejected claim 3.

Allowable Subject Matter

6.   Claims 5, 7-8, 13-15, and 21-23 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

7.   The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a data bit

counter having a width "w" comprising: an nth count bit has a value of gcount(n)' after an

active clock edge associated with the counter, and the logic includes determining

gcount(n)' using an XOR of a current count bit and at least one other bit in addition to all

limitations cited in preceding claims as seen in dependent claim 13 and further wherein

the at least one other bit as an AND of a previous count bit and a previous carry bit as

seen in dependent claims 5 and 21.

Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Allowance."

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

    a.   U.S. Patent No. 5,164,968 to Otto discloses a nine bit gray code generator.

    b.   U.S. Patent No. 5,191,425 to Hachiyama et al. disclose an image pickup apparatus

having a gray counter.

    c.   U.S. Patent No. 6,400,735 to Percey discloses a glitchless delay line using gray

code multiplexer.

    d.   U.S. Patent No. 6,434,642 to Camilleri et al. disclose a FIFO memory system and

method with improved determination of full and empty conditions and amount of data

stored.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The

examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

September 26, 2006